

## WHAT IS CLAIMED IS:

- 1                   1.     An optical logic circuit, comprising:  
2                             a substrate comprising of a first material; and  
3                             an optical layer overlaying the substrate at least  
4 partially comprising a second material, the optical layer configured to  
5 provide a plurality of optical pathways, at least one optical pathway  
6 configured to transmit an optical bias, at least one optical pathway  
7 configured to provide an optical input, and at least one optical pathway  
8 configured to provide an optical output,  
9                             wherein the optical pathways are configured to  
10 provide a Boolean logic output based on the at least one optical input.
- 1                   2.     The optical logic circuit of claim 1, further comprising:  
2                             an interference region configured to selectively cause  
3 interference of wavefronts of light entering the interference region.
- 1                   3.     The optical logic circuit of claim 2, wherein the  
2 interference region includes a first selective input, a bias input, and an  
3 interference region output.
- 1                   4.     The optical logic circuit of claim 3, wherein the  
2 interference region is configured to cause substantial cancellation of light  
3 exiting the interference region output when light is provided to the  
4 interference region through the first selective input.
- 1                   5.     The optical logic circuit of claim 3, wherein the  
2 interference region includes a second selective input.



1 12. The optical logic gate of claim 11, further comprising:  
2 at least two optical conduits configured to receive an  
3 optical input,  
4 wherein one of the optical inputs is an optical bias  
5 input.

1 13. The optical logic gate of claim 12, wherein the optical  
2 logic gate provides a Boolean NOT function.

1 14. The optical logic gate of claim 11, further comprising:  
2 at least three optical conduits configured to receive an  
3 optical input,  
4 wherein one of the optical inputs is an optical bias  
5 input.

1 15. The optical logic gate of claim 14, wherein the optical  
2 logic gate provides a Boolean NOT function.

1 16. The optical logic gate of claim 11, further comprising:  
2 an interference region coupled to at least two of the  
3 optical inputs and at least one of the optical outputs.

1 17. The optical logic gate of claim 11, wherein the first  
2 material comprises silicon (Si).

1 18. The optical logic gate of claim 11, wherein the second  
2 material comprises doped silicon (Si).

1 19. The optical logic gate of claim 11, wherein the first  
2 material comprises Gallium Arsenide (GaAs).

1 20. The optical logic gate of claim 11, wherein the second  
2 material comprises doped Gallium Arsenide (GaAs).

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1 21. The optical logic gate of claim 11, wherein the optical  
2 input is optically coupled to a Laser diode.

1 22. The optical logic gate of claim 11, wherein the optical  
2 input is optically coupled to a semiconductor diode.

1 23. A method of creating at least one optical logic gate,  
2 comprising;  
3 providing a substrate of a first material;  
4 providing a second material overlying the first material;  
5 patterning the second material by removing at least  
6 some of the second material; and  
7 providing a third material overlying at least the  
8 substrate.

1 24. The method of claim 23, wherein the second material  
2 is configured to provide pathways for the transmission of electromagnetic  
3 radiation within a predetermined wavelength spectrum.

1 25. The method of claim 23, wherein the third material is  
2 configured to provide pathways for the transmission of electromagnetic  
3 radiation within a predetermined wavelength spectrum.

1 26. The method of claim 23, further comprising:  
2 planarizing the third material.

1 27. The method of claim 23, further comprising:  
2 providing at least one optical input pathway and at  
3 least one optical output pathway of one of the second material and the  
4 third material.

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1                   28.    The method of claim 27, further comprising:  
2                               coupling an electromagnetic emitter to the at least one  
3   optical input pathway; and  
4                               coupling an electromagnetic detector to the at least  
5   one optical output pathway.

1                   29.    The method of claim 23, wherein the first material is  
2   substantially silicon.

1                   30.    The method of claim 23, wherein one of the second  
2   material and the third material is a doped silicon material.

1                   31.    A method of providing a Boolean logic optical output  
2   based on at least one optical input, comprising:  
3                               providing light to the at least one optical input;  
4                               providing a plurality of optical pathways;  
5                               providing a light; and  
6                               providing an optical output, the optical output based  
7   on the at least one input and representative of a Boolean logic function.

1                   32.    The method of claim 31, further comprising:  
2                               providing at least a portion of the plurality of optical  
3   pathways configured to selectively cause interference between of  
4   different wavefronts of light.

1                   33.    The method of claim 31, wherein the Boolean logic  
2   function is a NOT (inverter) gate.

1                   34.    The method of claim 31, wherein the Boolean logic  
2   function is a NOT AND (NAND) gate.

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35. The method of claim 31, wherein the Boolean logic function is configured of NOT (inverter) gates and Not AND (NAND) gates.

36. An optical logic circuit, comprising:  
a substrate comprising a first material; and  
an optical layer overlaying the substrate at least partially comprising a second material, the optical layer being patterned to provide a plurality of optical pathways, at least one optical pathway configured to provide an optical input, and at least one optical pathway configured to provide an optical output,  
wherein the optical pathways are configured to provide a Boolean logic output based on the at least one optical input.

37. The optical logic circuit of claim 36, further comprising:  
an interference region configured to selectively cause interference of wavefronts of light entering the interference region.

38. The optical logic circuit of claim 37, wherein the interference region includes a first selective input, a bias input, and an interference region output, the bias input transmitting an optical bias signal.

39. The optical logic circuit of claim 38, wherein the interference region is configured to cause substantial cancellation of light exiting the interference region output when light is provided to the interference region through the first selective input.

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1 40. The optical logic circuit of claim 38, wherein the  
2 interference region includes a second selective input.

1 41. The optical logic circuit of claim 40, wherein the  
2 interference region is configured to cause substantial cancellation of light  
3 exiting the interference region output when light is provided to the  
4 interference region through both the first selective input and the second  
5 selective input, and light is provided to neither of the first and second  
6 selective inputs.

1 42. The optical logic circuit of claim 36, wherein the  
2 Boolean logic output is representative of the NOT (inverter) function.

1 43. The optical logic circuit of claim 36, wherein the  
2 Boolean logic output is representative of the NOT AND (NAND) function.

1 44. The optical logic circuit of claim 36, having a  
2 multiplicity of optical logic gates configured to function as an optical  
3 processor.

1 45. The optical logic circuit of claim 44, wherein the  
2 optical processor is configured of NOT (inverter) gates and NOT AND  
3 (NAND) gates.

1 46. The optical logic circuit of claim 36, wherein the  
2 Boolean logic output is representative of the XOR (exclusive OR) function.